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Question Paper Code : 30958

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Sixth/Eighth Semester

Electronics and Communication Engineering

EC 2354 — VLSI DESIGN

(Common to Biomedical Engineering)

(Regulation 2008)

(Also common to PTEC 2354 — VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Determine the drain current of short channel NMOS transistor for the following measurements : $V_{DS} = 1.5$ V, $V_{GS} = 2$ V, $V_{BS} = 0$ V, $V_{TO} = 0.43$ V. Assume $V_{DSAT} = 0.6$ V, $K'_n = 110$ uA/V^2, $\lambda = 0.1$ V^{-1}, $\gamma = 0.4$ and $W/L = 0.4/0.25$.

2. Write down any two Layout design rules.

3. Define power dissipation.

4. Mention the types of scaling.

5. List the various power losses in CMOS circuits.

6. Enumerate the features of synchronizers.

7. State the need for testing.

8. State the principle behind manufacturing testing.

9. Write the Verilog module for a 1-bit full adder.

10. Give an example for implicit continuous assignment.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the electrical properties of MOS transistor in detail.

Or

(b) Derive an expression for V_{in} of a CMOS inverter to achieve the condition $V_{in} = V_{out}$. What should be the relation for $\beta_n = \beta_p$?

12. (a) (i) Explain in detail about the scaling concept and reliability concept. (8)

(ii) Describe in detail about the transistor sizing for the performance in combinational networks. (8)

Or

(b) Discuss in detail about the resistive and capacitive delay estimation of a CMOS inverter circuit. (16)

13. (a) (i) Consider the circuit of Figure 13 (a) (i). (8)

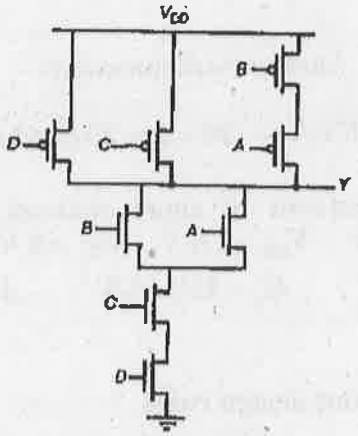

Figure 13 (a) (i)

(1) What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

(2) What are the input patterns that give the worst case t_{pHL} and t_{pLH}? State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

(3) Determine the dynamic power dissipation in the logic gate. Assume $V_{DD} = 2.5$ V, $C_{out} = 30\,fF$ and $fclk = 250$ MHz.

(ii) Show that the output logic level of pseudo NMOS logic is dependent on the size of the transistor. (4)

(iii) List out the issues present in dynamic CMOS logic design. Explain any two. (4)

Or

(b) (i) Consider the circuit shown in Fig. 13 (b) (i).

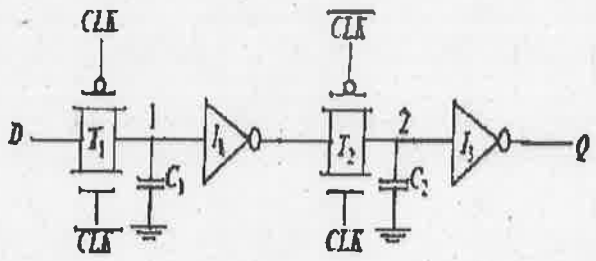

Fig. 13 (b) (i)

(1) State whether the circuit is a latch or edge triggered register. Justify your answer.

(2) In the circuit consider C1 and C2 as the intrinsic capacitances of inverters and transmission gates. Assuming ideal clock, compute the setup time, hold time and propagation delay in terms of the inverter I1, I2 delay and transmission gate T1, T2 delay. (8)

(ii) Explain the true single phase clock latch. (8)

14. (a) Explain Boundary Scan testing.

Or

(b) Explain logic verification in detail.

15. (a) (i) Draw an active high 2/4 decoder using NOR gates and write the Verilog gate level description. (8)

(ii) Describe the three ways of specifying delays in continuous assignment statements. (8)

Or

(b) (i) Write the data flow modeling for a 4 to 1 MUX using Verilog HDL. (8)

(ii) Explain the different timing controls available in Verilog HDL. (8)